

REMARKS

Claims 34-37 have been added without introducing new matter.

Claim Rejections - 35 U.S.C. §102

Claims 1-7 and 10-33 are rejected, under 35 U.S.C. 102(e), as allegedly being anticipated by Chen et al. US Patent 6,757,882 (hereinafter Chen).

Applicants respectfully traverse in view of the following.

Independent Claim 1 recites a limitation whereby in response to a selection of the selectable user module, a description of a hardware resource requirement of the selectable user module is compared with a description of the plurality of programmable hardware resources, as claimed. Moreover, independent Claim 1 recites graphically corresponding the first allowed programmable hardware resource to the selectable user module, as claimed.

In contrast, Chen discloses a list of available memory items that can be selected/added (see Chen, col. 14, lines 20-30). The rejection equates a list of memory items as disclosed by Chen to the user module, as claimed. Moreover, the rejection relies on Chen disclosing that when a processor is chosen, it is first determined whether processor supports the bus architecture on chip bus specification and connects the processor high performance peripherals, on-chip memory and interface functions (see Chen, col. 12, lines 31-45). Chen further discloses that once the type of bus is determined, all the main system components that support the processor specification will be determined based on the information stored in the database and presented to the user for selection (see Chen, col. 12, lines 45-48).

Accordingly, the memory item is selected after determining the compatibility of the processor and the bus architecture. As presented above, the rejection equates the list of memory items to user module, as claimed. As such, Chen fails to teach or suggest in response to a selection of the selectable user module, comparing a description of a hardware resource requirement of the selectable user module with a description of the plurality of programmable hardware resources, as claimed. Moreover, Chen teaches away from the recited limitation by disclosing that the memory item is selected after determining the compatibility of the processor and the bus architecture.

Furthermore, Applicants respectfully wish to remind the Examiner that “[a]nticipation requires the disclosure in a single prior art reference of each claim under consideration” (W.L. Gore & Assocs. v. Garlock Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983)). However, it is not sufficient that the reference recite all the claimed elements. As stated by the Federal Circuit, the prior art reference must disclose each element of the claimed invention “arranged as in the claims” (emphasis added; Lindermann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)).

Independent Claim 1 recites displaying a selectable user module and in response to the selection of the selectable user module, comparing a description of a hardware resource requirement of the selectable user module with a description of the plurality of programmable hardware resources associated with the programmable integrated circuit, as claimed. As discussed and presented above, the selection of memory items is after determining the compatibility of the processor and the bus architecture. Moreover, Applicants respectfully remind the Examiner that the selection of memory items as disclosed by Chen is in column

14 and determining the compatibility of the processor is in column 12. As such, the elements of the recited limitations as disclosed by Chen are not arranged as in the Claim 1 whereby in response to a selection of a user module, comparing descriptions, as claimed. Therefore, Chen not only fails to teach or suggest but Chen explicitly teaches away from comparing a description of a hardware resource requirement of the selectable module with a description of the plurality of programmable hardware resources in response to a selection of the selectable user module, as claimed.

Moreover, as discussed above Chen discloses selecting various components (e.g., processor, memory list and etc.) and determining compatibility of a processor for example. However, Chen fails to teach or suggest graphically corresponding the first allowed programmable hardware resource to the selectable user module, as claimed.

Accordingly, Chen fails to anticipate independent Claim 1, under 35 U.S.C. 102(e). Moreover, independent Claims 15, 18 and 26 recite limitations similar to that of independent Claim 1 and are patentable over Chen for similar reasons. Dependent claims are patentable by virtue of their dependency.

As per Claims 4 and 6, the rejection relies on Chen disclosing that upon determining the information bus, compatibility analyzer stores the supported bus architecture information, including related synthesized information into database. Moreover, the rejection relies on Figure 6 to show highlighting the first allowed programmable hardware resource, as claimed. Applicants respectfully submit that Figure 6 shows a plurality of selectable options (e.g., operating system) and that in response to the selection of an option, the option may be highlighted (see

Chen Figure 6). In contrast, Claim 4 recites highlighting the first allowed programmable hardware resource, as claimed which is in response to the comparing of description and not in response to a selection of an option as disclosed by Chen. As such, Chen fails to teach or suggest highlighting, as recited in the claimed fashion.

As per Claims 10, 11 and 13, Chen discloses that customizable attribute description set forth between customizable attribute description tags may include a number of IP component parameters, identification of the IP component parameters, the manner of resolution and user prompts (see Chen, col. 9, lines 18-26). Applicants do not understand customizable attribute description tags, that may allow matching various components, to teach or suggest updating the description, as claimed.

As per Claims 12 and 14, Chen discloses that customizable attribute description set forth between customizable attribute description tags may include a number of IP component parameters, identification of the IP component parameters, the manner of resolution and user prompts as discussed and presented above. Applicants respectfully submit that a disclosure that a description tag may include a number of parameters differs from adding an additional module/chip description, as claimed. Adding additional information, as claimed is after the original set has been generated whereas a disclosure that a description tag may include a number of parameters that may or may not have been added after the original set was generated. As such, Chen fails to explicitly disclose adding additional module/chip description, as claimed.

Other dependent claims recite limitations similar to the limitations presented and discussed above and are patentable over Chen for similar reasons. As such, allowance of Claims 1-7 and 10-33 is earnestly solicited.

Claim Rejections - 35 U.S.C. §103

Claims 8 and 9 are rejected, under 35 U.S.C. §103, as being allegedly obvious over Chen in view of PSoC Designer: Integrated Development Environment User Guide Revision 1.09 (hereinafter Guide 1.09). Applicants respectfully traverse in view of the following.

Claims 8-9 depend from independent Claim 1 and are patentable over Chen for reasons similar to that of independent Claim 1. Applicants do not understand Guide 1.09 to remedy the failures of Claim 1 as presented and as discussed above. As such, the combination of Chen and Guide 1.09 fails to render Claims 8-9 obvious, under 35 U.S.C. 103(a). As such, allowance of Claims 8-9 is earnestly solicited.

For the above reasons, the Applicants request reconsideration and withdrawal of the rejections under 35 U.S.C. §102 and 35 U.S.C. §103.

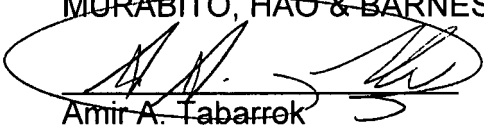
CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-33 and newly added Claims 34-37 overcome the rejections of record and, therefore, allowance of Claims 1-37 is earnestly solicited.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Dated: April 26th, 2007

Respectfully submitted,
MURABITO, HAO & BARNES LLP



Amir A. Tabarrek
Registration No. 57,137

MURABITO, HAO & BARNES LLP
Two North Market Street
Third Floor
San Jose, California 95113

(408) 938-9060 Voice
(408) 938-9069 Facsimile